CERTIFICATE

I, Takumi SASAKI, residing at 1-11-11, Higashi-oowada, Ichikawa-shi, Chiba-ken, 272-0026 Japan, hereby certify that I am the translator of the attached document, namely a Certified Copy of Japanese Patent Application No. 2002-209880 and certify that the following is a true translation to the best of my knowledge and belief.

Takumi Sasaki — December 14, 2005

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[Title of the Invention] ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

[Claims]

[Claim 1] An electro-optical device comprising:

a first electrode group including first electrodes arranged in a matrix;

light-emitting layers lying on the first electrodes;

a second electrode lying over the light-emitting layers;

power supply lines, connected to the first electrodes, for supplying currents to the light-emitting layers; and

a cathode line, connected to the second electrode, having an area larger than the sum of the areas of the power supply lines.

[Claim 2] The electro-optical device according to Claim 1, wherein the cathode line has a portion having a width larger than that of the power supply lines.

[Claim 3] The electro-optical device according to Claim 1, wherein the width of the entire cathode line is larger than that of the power supply lines.

[Claim 4] The electro-optical device according to Claim 1, wherein the light-emitting layers emit different color lights and include a plurality of types of light-emitting elements disposed between the first electrodes and the

second electrode and the power supply lines are connected to the light-emitting elements depending on the type.

[Claim 5] The electro-optical device according to Claim 4, wherein the cathode line has a width larger than that of the power supply lines connected to the light-emitting elements depending on the type.

[Claim 6] The electro-optical device according to any one of Claims 1 to 5, further comprising:

an effective display region formed by the first electrode group; and

a dummy region which is located outside the effective display region and which is not used to display an image,

wherein the power supply lines and the cathode line are arranged around the dummy region.

[Claim 7] The electro-optical device according to Claim 6, wherein the second electrode covers at least the effective region and the dummy region.

[Claim 8] The electro-optical device according to Claim 7, wherein the whole of the cathode line is connected to the second electrode.

[Claim 9] The electro-optical device according to any one of Claims 6 to 8, further comprising:

switching elements connected to the first electrodes; and

control lines for controlling the switching elements,

wherein the control lines are arranged such that at least three sides of each control line are surrounded by the power supply lines and the cathode line.

[Claim 10] The electro-optical device according to Claim 9, wherein the control lines include scanning lines for scanning the switching elements and also include signal lines for transmitting image signals to the switching elements.

[Claim 11] The electro-optical device according to any one of Claims 1 to 10, wherein the light-emitting elements include hole injection/transport layers and the light-emitting layers made of an organic electroluminescent material, these layers being stacked.

[Claim 12] An electronic apparatus comprising the display element according to any one of Claims 1 to 11.

[0001]

[Technical Field of the Invention]

The present invention relates to electro-optical devices and electronic apparatuses. The present invention particularly relates to an electro-optical device comprising an organic electroluminescent material and also relates to an electronic apparatus including such an electro-optical device.

[0002]

[Description of the Related Art]

In recent years, the following apparatuses have been developed: color electro-optical apparatuses including light-emitting elements which are disposed between pixel electrodes (anodes) and cathodes and which are made of luminescent materials. In particular, organic EL apparatuses containing organic electroluminescent (organic EL) materials, which are luminescent materials, have been developed. A known electro-optical apparatus (organic EL apparatus) will now be briefly described.

[0003]

FIG. 12 is a wiring diagram of the known electro-optical device. With reference to FIG. 12, the known electro-optical device includes a plurality of scanning lines 901, a plurality of signal lines 902 extending to intersect the scanning lines 901, a plurality of luminescent power-supply lines 903 extending in parallel to the signal lines 902, and pixel regions A each placed adjacent to corresponding intersects of the scanning lines 901 and the signal lines 902. The signal lines 902 are connected to a data side-driving circuit 904 including a shift register, a level shifter, a video line, and an analog switch. The scanning lines 901 are connected to a scanning side-driving circuit 905 including a shift register and a level shifter.

[0004]

The pixel regions A include switching thin-film

transistors 913 having gate electrodes for receiving scanning signals transmitted through the scanning lines 901, hold capacitors Cap for holding pixel signals transmitted from the signal lines 902 through the switching thin-film transistors 913, current thin-film transistors 914 having gate electrodes for receiving the pixel signals held in the hold capacitors Cap, pixel electrodes 911 into which driving currents flow through the luminescent power-supply lines 903 when the pixel electrodes 911 are electrically coupled with the luminescent power-supply lines 903 with the current thin-film transistors 914, and light-emitting layers 910 sandwiched between the pixel electrodes 911 and a cathode 912. The cathode 912 is connected to cathodic power supply circuits 931.

[0005]

The light-emitting layers 910 include three types of light-emitting layers: light-emitting layers 910R for emitting red light, light-emitting layers 910G for emitting green light, and light-emitting layers 910B for emitting blue light. The light-emitting layers 910R, 910G, and 910B are arranged in a striped pattern. Luminescent power-supply lines 903R, 903G, and 903B are connected to the light-emitting layers 910R, 910G, and 910B, respectively, with the current thin-film transistors 914 and also connected to luminescent power-supply circuits 932. The reason why the

luminescent power-supply lines are each connected to the corresponding color light-emitting layers is that the light-emitting layers 910 are driven with different voltages depending on color.

[0006]

In the above configuration, when scanning signals are supplied to the scanning lines 901 and the switching thin-film transistors 913 are therefore turned on, charges corresponding to image signals are held in the hold capacitors Cap. The current thin-film transistors 914 are turned on or off depending on the amount of the charges held in the hold capacitors Cap. Currents are applied to the pixel electrodes 911 through the luminescent power-supply lines 903R, 903G, and 903B with the current thin-film transistors 914 and driving currents are then applied to the cathode 912 through the light-emitting layers 910. This allows the light-emitting layers 910 to emit light of which the amount depends on the amount of the currents flowing through the light-emitting layers 910.

[0007]

[Problems to be Solved by the Invention]

As described above, in the known electro-optical apparatus, the luminescent power-supply circuits 932 are individually connected to the light-emitting layers 910R for emitting red light, the light-emitting layers 910G for

emitting green light, and the light-emitting layers 910B for emitting blue light such that driving currents are applied to the light-emitting layers 910R, 910G, and 910B through the luminescent power-supply lines 903R, 903G, and 903B, respectively. This is because the light-emitting layers 910 are driven with different voltages depending on color.

[0008]

The cathode 912 connected to the light-emitting layers 910 is common to the light-emitting layers 910. This is because the cathode 912 is used to recover the current applied to the light-emitting layers 910 and need not be divided depending on color unlike the luminescent power-supply lines 903.

[0009]

The cathode 912 is used as a member for adjusting the reference voltage applied to the luminescent power-supply lines 903 and must therefore be equipotential as a whole. However, since the currents applied to all the light-emitting layers 910R, 910G, and 910B flow into the cathode 912, the sum of the currents flowing into the cathode 912 is larger than that of the currents flowing through the luminescent power-supply lines 903R, 903G, and 903B.

[0010]

Therefore, if the cathode 912 has a small wiring resistance, a serious voltage drop occurs due to the wiring

resistance; hence, portions of the cathode 912 have different potentials. If the difference in potential is large, predetermined currents cannot be applied to the pixel regions A. This causes a problem in that a normal image cannot be displayed but an uneven image or a low-contrast image is displayed.

[0011]

The present invention has been made in view of the foregoing circumstances. It is an object of the invention to provide an electro-optical device in which a wrong image, for example, a low-contrast image, can be prevented from being displayed in such a manner that image signals are constantly supplied by minimizing the voltage drop due to the wiring resistance of a cathode and to provide an electronic apparatus including the electro-optical device.

[0012]

[Means for Solving the Problems]

In order to achieve the above object, an electro-optical device according to the invention includes a first electrode group including first electrodes arranged in a matrix; light-emitting layers lying on the first electrodes; a second electrode lying over the light-emitting layers; power supply lines, connected to the first electrodes, for supplying currents to the light-emitting layers; and a cathode line, connected to the second electrode, having an

area larger than the sum of the areas of the power supply lines.

According to the invention, since cathode line has an area larger than the sum of the areas of the power supply lines such that the cathode line has a small wiring resistance, the voltage drop in the cathode line can be reduced when currents supplied from the power-supply lines to light-emitting elements through the first electrodes flow in the cathode line. Therefore, image signals can be reliably transmitted such that a wrong image such as a low-contrast image is prevented from being displayed.

In the electro-optical device, the cathode line has a portion having a width larger than that of the power supply lines.

According to the invention, since the cathode line has at least one portion having a width larger than that of the power supply lines and has an area larger than the sum of the areas of the power supply lines, the portion can be located at any position depending on the arrangement of the power supply lines, the cathode line, and other lines.

In the electro-optical device, the width of the entire cathode line is larger than that of the power supply lines.

According to the invention, the width of the entire cathode line is larger than that of the power supply lines. This is extremely effective in reducing the wiring

resistance in the cathode line.

In the electro-optical device, the light-emitting layers emit different color lights and include a plurality of types of light-emitting elements disposed between the first electrodes and the second electrode and the power supply lines are connected to the light-emitting elements depending on the type.

In the electro-optical device, the cathode line has a width larger than that of the power supply lines connected to the light-emitting elements depending on the type.

According to the invention, since the cathode line has an area larger than that of each of the power supply lines although the light-emitting elements are arranged and the power supply lines are connected to the light-emitting elements depending on the type, a voltage drop causing a wrong image can be prevented from occurring in the cathode line even if currents supplied to the light-emitting elements through the power supply lines flow into the a cathodic power supply.

The electro-optical device further includes an effective display region formed by the first electrode group and a dummy region which is located outside the effective display region and which is not used to display an image. The power supply lines and the cathode line are arranged around the dummy region.

In the electro-optical device, the second electrode covers at least the effective region and the dummy region.

In the electro-optical device, the whole of the cathode line is connected to the second electrode.

According to the invention, since the whole of the cathode line is connected to the second electrode, the resistance of connections can be reduced. This is extremely effective in preventing a wrong image from being displayed.

The electro-optical device further includes switching elements connected to the first electrodes and also includes control lines for controlling the switching elements. The control lines are arranged such that at least three sides of each control line are surrounded by the power supply lines and the cathode line.

According to the invention, since at least three sides of each control line to which a high-frequency control signal for controlling the operation of each switching element is supplied are surrounded by the power supply lines and the cathode line, noise contained in the control signal can be reduced. This is extremely effective in preventing a wrong image from being displayed.

In the electro-optical device, the control lines include scanning lines for scanning the switching elements and also include signal lines for transmitting image signals to the switching elements.

In the electro-optical device, the light-emitting elements include hole injection/transport layers and the light-emitting layers made of an organic electroluminescent material, these layers being stacked.

According to the invention, since the hole injection/transport layers and the light-emitting layers are stacked, a bright image with a correct color can be displayed in such a manner that driving currents with less voltage fluctuations are applied to the light-emitting layers and the voltage drop in the cathode line is reduced.

An electronic apparatus of the invention includes the electro-optical device described above.

[0013]

[Description of the Embodiments]

An electro-optical device and electronic apparatus according to an embodiment of the present invention will now be described in detail with reference to the attached drawings. In the following drawings, in order to show each layer and member in the drawings on a recognizable scale, different scales are used to show the layers and members. FIG. 1 is a schematic view showing a wiring structure of the electro-optical device according to the embodiment of the present invention.

[0014]

The electro-optical device 1 shown in FIG. 1 is an

active matrix-type organic EL device including thin-film transistors (Thin Film Transistors) serving as switching elements. As shown in FIG. 1, the electro-optical device 1 of this embodiment includes a plurality of scanning lines 101, a plurality of signal lines 102 extending to intersect the scanning line 101, a plurality of luminescent power-supply lines 103 extending in parallel to the signal lines 102, pixel regions A disposed near the intersections of the scanning lines 101 and signal lines 102. The scanning lines 101 and signal lines 102 are herein defined as parts of control lines.

[0015]

The signal lines 102 are connected to a data side-driving circuit 104 including a shift register, a level shifter, video lines, and analogue switches. The signal lines 102 are also connected to an inspection circuit 106 including thin-film transistors. The scanning lines 101 are connected to scanning side-driving circuits 105 including a shift register and a level shifter.

[0016]

The pixel regions A contain switching thin-film transistors 112, hold capacitors Cap, current thin-film transistors 123, pixel electrodes (first electrodes) 111, light-emitting layers 110, and a cathode (second electrode) 12. The switching thin-film transistors 112 and the current

thin-film transistors 123 correspond to so-called switching elements. The switching thin-film transistors 112 include gate electrodes connected to the scanning lines 101 and are turned on or off depending on scanning signals transmitted from the scanning line 101. The hold capacitors Cap hold pixel signals transmitted from the signal lines 102 via the switching thin-film transistors 112.

[0017]

The current thin-film transistors 123 includes gate electrodes connected to the switching thin-film transistors 112 and the Hold capacitors Cap. The pixel signals held in the Hold capacitors Cap are transmitted to these gate electrodes. The pixel electrodes 111 are connected to the current thin-film transistors 123 and driving currents are applied to the pixel electrodes 111 from the luminescent power-supply lines 103 when the pixel electrodes 111 are electrically coupled with the luminescent power-supply lines 103 with the current thin-film transistors 123 disposed therebetween. The light-emitting layers 110 are sandwiched between the pixel electrodes 111 and the cathode 12.

[0018]

The light-emitting layers 110 include three types of layers: light-emitting layers 110R for emitting red light, light-emitting layers 110G for emitting green light, and light-emitting layers 110B for emitting blue light. The

light-emitting layers 110R, 110G, and 110B are arranged in a striped pattern. Luminescent power-supply lines 103R, 103G, and 103B are connected to the light-emitting layers 110R, 110G, and 110B, respectively, with the current thin-film transistors 123 and also connected to luminescent power-supply circuits 132. Since the light-emitting layers 110R, 110G, and 110B are driven with different voltages depending on color, the luminescent power-supply lines 103R, 103G, and 103B are arranged depending on color.

[0019]

In the electro-optical device of this embodiment, first capacitors C_1 are disposed between the cathode 12 and the luminescent power-supply lines 103R, 103G, and 103B. When the electro-optical device is driven, charges are stored in the first capacitors C_1. When the potentials of driving currents flowing in the luminescent power-supply lines 103 fluctuate during the operation of the electro-optical device 1, the stored charges are discharged to the luminescent power-supply lines 103, thereby reducing the fluctuation in the potentials of the driving currents. This allows the electro-optical device 1 to display a normal image.

[0020]

In the electro-optical device 1, when scanning signals are transmitted to the switching thin-film transistors 112 from the scanning lines 101 and the switching thin-film

transistors 112 are therefore turned on, the potentials of the signal lines 102 are held in the capacitors Cap. The current thin-film transistors 123 are turned on or off depending on the potentials held in the capacitors Cap. Driving currents are applied to the pixel electrodes 111 from the luminescent power-supply lines 103R, 103G, and 103B via channels of the current thin-film transistors 123 and currents are applied to the cathode 12 via the light-emitting layers 110R, 110G, and 110B. In this operation, the light-emitting layers 110 emit lights of which the amounts depend on the amounts of currents flowing in the light-emitting layers 110.

[0021]

A configuration of the electro-optical device 1 according to this embodiment will now be described in detail with reference to FIGS. 2 to 4. FIG. 2 is a schematic plan view showing the electro-optical device of this embodiment, FIG. 3 is a sectional view taken along the line A-A' of FIG. 2, and FIG. 4 is a sectional view taken along the line B-B' of FIG. 2. As shown in FIG. 2, the electro-optical device 1 of this embodiment includes a substrate 2; a pixel electrode group region which is not shown; the luminescent power-supply lines 103 (103R, 103G, and 103B); and a display pixel section 3 (the section surrounded by the dotted-chain line in the figure).

[0022]

The substrate 2 is a transparent substrate made of, for example, glass. The pixel electrode group region contains the pixel electrodes (not shown) which are connected to the current thin-film transistors 123 shown in FIG. 1 and which are arranged on the substrate 2 in a matrix. As shown in FIG. 2, the luminescent power-supply lines 103 (103R, 103G, and 103B) are arranged around the pixel electrode group region and each connected to the corresponding pixel electrodes as shown in FIG. 2. The display pixel section 3 is disposed above at least the pixel electrode group region and has substantially a rectangular shape when viewed from above. The display pixel section 3 is partitioned into an actual display region 4 (the region surrounded by the two-dot chain line in the figure) placed at the center area and a dummy region 5 (the region between the dotted line and the two-dot line) placed around the actual display region 4 (this region may be referred to as an effective display region).

[0023]

In the figure, the scanning driving circuits 105 described above are disposed at both sides of the actual display region 4. The scanning driving circuits 105 are placed below the dummy region 5 (on the side close to the substrate 2). Furthermore, scanning line-driving circuit

control signal lines 105a and scanning line-driving circuit power-supply lines 105b connected to the scanning driving circuits 105 are placed below the dummy region 5. The inspection circuit 106 is disposed above the actual display region 4. The inspection circuit 106 placed below the dummy region 5 (on the side close to the substrate 2). The quality and defects of the electro-optical device 1 can be checked using the inspection circuit 106 during the manufacture thereof or at the time of the delivery thereof.

[0024]

As shown in FIG. 2, the luminescent power-supply lines 103R, 103G, and 103B are arranged around the dummy region 5. The luminescent power-supply lines 103R, 103G, and 103B extend upward from the lower side of the substrate 2 along the scanning line-driving circuit power-supply lines 105b, bend at the positions that the scanning line-driving circuit power-supply lines 105b terminate, further extend along the outside of the dummy region 5, and are connected to the pixel electrodes which are not shown disposed in the actual display region 4. The substrate 2 has a cathode line 12a connected to the cathode 12. The cathode line 12a has substantially a C shape when viewed from above and surrounds the luminescent power-supply lines 103R, 103G, and 103B.

[0025]

The actual display region 4 and the dummy region 5 are

surrounded by the cathode line 12a and the luminescent power-supply lines 103R, 103G, and 103B. In the actual display region 4, a plurality of the scanning lines 101 shown in FIG. 1 are arranged and the signal lines 102 are arranged such that the signal lines 102 and the scanning lines 101 intersect. That is, the scanning lines 101 and the signal lines 102 are arranged in an area on the substrate 2, the area being surrounded by the cathode line 12a and the light-emitting power-supply lines 103R, 103G, and 103B on three sides.

[0026]

The cathode line 12a and the luminescent power-supply lines 103R, 103G, and 103B, which are characteristic of the present invention, will now be described. As shown in FIG. 1, currents applied from the luminescent power-supply lines 103R, 103G, and 103B to the light-emitting layers 110 flow into the cathode 12 (the cathode line 12a). Thus, if the cathode line 12a, of which the width is limited, has a wiring resistance, a serious voltage drop is caused. Therefore, the voltage varies depending on the position of the cathode line 12a, thereby causing the display of a wrong image a such as a low-contrast image.

[0027]

In this embodiment, in order to prevent such a problem, the cathode line 12a has an area larger than that of each of

the luminescent power-supply lines 103R, 103G, and 103B. In order to reduce the wiring resistance, the cathode line 12a preferably has a large area. However, the area of the cathode line 12a is limited to a certain extent because various wiring lines are arranged on the substrate 2 as shown in FIG. 2.

[0028]

On the assumption that the luminescent power-supply lines 103R, 103G, and 103B and the cathode line 12a have the same resistance per unit length in the longitudinal direction, the cathode line 12a is designed to have at least one portion having a width larger than that of the luminescent power-supply lines 103R, 103G, and 103B and the cathode line 12a therefore has an area larger than that of each of the luminescent power-supply lines 103R, 103G, and 103B. In the configuration shown in FIG. 2, the entire cathode line 12a has a width larger than that of each of the luminescent power-supply lines 103R, 103G, and 103B.

[0029]

Suppose that the same voltage is applied to the luminescent power-supply lines 103R, 103G, and 103B; the luminescent power-supply lines 103R, 103G, and 103B have the same width; the same current flows in the luminescent power-supply lines 103R, 103G, and 103B; and all the light-emitting layers 110 have the same electric properties.

Currents flowing in the light-emitting layers 110 and the luminescent power-supply lines 103R, 103G, and 103B flow into the cathode line 12a. Thus, in order to that the voltage drop in the cathode line 12a is substantially equal to the voltage drops in the luminescent power-supply lines 103R, 103G, and 103B, the cathode line 12a preferably has a width larger than the sum of the widths of the luminescent power-supply lines 103R, 103G, and 103B.

[0030]

However, in the electro-optical device of this embodiment, the light-emitting layers 110 have different properties depending on color; different voltages are applied to the luminescent power-supply lines 103R, 103G, and 103B depending on color; and therefore different currents flow. Therefore, in this embodiment, the cathode line 12a preferably has a width larger than that of one of the luminescent power-supply lines to which the largest voltage is applied and in which the largest current flows (that is, the largest voltage drop is caused). The other luminescent power-supply lines are formed so as to have a smaller width because smaller voltages are applied thereto and therefore smaller currents flow therein.

[0031]

Thus, the cathode line 12a has a width larger than that of the luminescent power-supply lines 103R, 103G, and 103B.

The cathode line 12a and the luminescent power-supply lines 103R, 103G, and 103B are designed as described above. In the configuration shown in FIG. 2, the entire cathode line 12a has a width larger than that of the luminescent power-supply lines 103R, 103G, and 103B. However, the cathode line 12a may have at least one portion having a width larger than that of the luminescent power-supply lines 103R, 103G, and 103B depending on the arrangement of the lines.

[0032]

As shown in FIG. 2, a polyimide tape 130 is attached to one end of the substrate 2 and a control IC 131 is mounted on the polyimide tape 130. The control IC 131 includes the data-side driving circuit 104 shown in FIG. 1, a cathodic power supply circuit 131, and the luminescent power-supply circuits 132.

[0033]

As shown in FIGS. 3 and 4, a circuit section 11 is disposed on the substrate 2 and the display pixel section 3 is disposed on the circuit section 11. The substrate 2 includes a sealing member 13 surrounding the display pixel section 3 and a sealing substrate 14 is disposed above the display pixel section 3. The sealing substrate 14 is joined to the substrate 2 with the sealing member 13 disposed therebetween. The sealing substrate 14 is made of glass, metal, resin, or the like. An adsorbent 15 is attached to

the rear face of the sealing substrate 14 and adsorbs moisture or oxygen present in a space between the display pixel section 3 and the sealing substrate 14. A getter may be used instead of the adsorbent 15. The sealing member 13 is made of, for example, a thermosetting resin or an ultraviolet-setting resin, and is preferably made of an epoxy resin, which is one of thermosetting resins, in particular.

[0034]

A pixel electrode group region 11a is disposed at a center area of the circuit section 11. The pixel electrode group region 11a contains the current thin-film transistors 123 and the pixel electrodes 111 connected to the current thin-film transistors 123. The current thin-film transistors 123 are disposed below a base-protecting layer 281, a second interlayer-insulating layer 283, and a first interlayer-insulating layer 284 arranged on the substrate 2. The pixel electrodes 111 are disposed on the first interlayer-insulating layer 284. Electrodes (source electrodes) which are connected to the current thin-film transistors 123 and which are disposed on the second interlayer-insulating layer 283 are connected to the luminescent power-supply lines 103 (103R, 103G, or 103B). The circuit section 11 contains the capacitors Cap and the switching thin-film transistors 112, which are not shown in

FIGS. 3 and 4. The signal lines 102 are also not shown in FIGS. 3 and 4. Furthermore, the switching thin-film transistors 112 and the current thin-film transistors 123 are not shown in FIG. 4.

[0035]

As shown in FIG. 3, the scanning driving circuits 105 are disposed on both sides of the pixel electrode group region 11a. As shown in FIG. 4, the inspection circuit 106 is disposed on the left side of the pixel electrode group region 11a. The scanning driving circuits 105 include n- or p-channel type thin-film transistors 105c that are components of an inverter included in the shift register. The thin-film transistors 105c have the same configuration as that of the current thin-film transistors 123 except that the thin-film transistors 105c are not connected to the pixel electrodes 111. The inspection circuit 106 includes thin-film transistors 106a. The thin-film transistors 106a have the same configuration as that of the current thin-film transistors 123 except that the thin-film transistors 106a are not connected to the pixel electrodes 111.

[0036]

As shown in FIG. 3, the scanning line-driving circuit control signal lines 105a are disposed on the base-protecting layer 281 located outside the scanning driving circuits 105. Furthermore, the scanning line-driving

circuit power-supply lines 105b are disposed on the second interlayer-insulating layer 283 located outside the scanning line-driving circuit control signal lines 105a. As shown in FIG. 4, the inspection-circuit control signal line 106b is disposed on the base-protecting layer 281 located on the left side of the inspection circuit 106. Furthermore, the inspection-circuit power-supply line 106c is disposed on the second interlayer-insulating layer 283 located on the left side of the inspection-circuit control signal line 106b. The luminescent power-supply lines 103 are disposed outside the scanning line-driving circuit power-supply lines 105b. The luminescent power-supply lines 103 have a double wiring structure consisting of two-types of lines and are arranged outside the display pixel section 3 as described above. The use of the double wiring structure leads to a reduction in resistance.

[0037]

For example, one of the red luminescent power-supply lines 103R that is located in a left area of FIG. 3 includes a first line $103R_1$ disposed on the base-protecting layer 281 and a second line $103R_2$ disposed above the first line $103R_1$ with the second interlayer-insulating layer 283 disposed therebetween. As shown in FIG. 2, the first line $103R_1$ is connected to the second line $103R_2$ with a contact hole $103R_3$ extending through the second interlayer-insulating layer 283.

The first line $103R_1$ and the cathode line 12a are disposed on the same level and the second interlayer-insulating layer 283 lies between the first line $103R_1$ and the cathode line 12a. As shown in FIGS. 3 and 4, the cathode line 12a is electrically connected to a cathode line 12b, disposed on the second interlayer-insulating layer 283, with a contact hole. That is, the cathode line 12a also has a double wiring structure. The second line $103R_2$ and the cathode line 12b are disposed on the same level and the first interlayer-insulating layer 284 lies between the second line $103R_2$ and the cathode line 12b. According to such a configuration, second capacitors C_2 are disposed between the first line $103R_1$ and the cathode line 12a and also disposed between the second line $103R_2$ and the cathode line 12b.

[0038]

The blue and green luminescent power-supply lines 103G and 103B located in a right area of FIG. 3 also have a double wiring structure. The green and blue luminescent power-supply lines 103G and 103B include first lines $103G_1$ and $103B_1$, respectively, disposed on the base-protecting layer 281 and also include second lines $103G_2$ and $103B_2$, respectively, disposed on the second interlayer-insulating layer 283. As shown in FIGS. 2 and 3, the first lines $103G_1$ and $103B_1$ are connected to the second lines $103G_2$ and $103B_2$ with contact hole $103G_3$ and $103B_3$, respectively, extending

through the second interlayer-insulating layer 283. The second capacitors C_2 are disposed between the blue first line $103B_1$ and the cathode line 12a and also disposed between the blue second line $103B_2$ and the cathode line 12b.

[0039]

The distance between the first and second lines $103R_1$ and $103R_2$ is preferably 0.6 to 1.0 μm. When the distance is smaller than 0.6 μm, the parasitic capacitance between source metals and gate metals, as well as the signal lines 102 and the scanning lines 101, having different potentials is large. This is not preferable. For example, in the actual display region 4, there are many crossover sites of the source metals and gate metals. Therefore, there is a problem in that the sites can cause a time delay between image signals if the sites have a large parasitic capacitance. Thus, the image signals cannot be written in the pixel electrodes 111 in a predetermined period, thereby causing low contrast. The second interlayer-insulating layer 283 disposed between the first and second lines $103R_1$ and $103R_2$ is preferably made of, for example, SiO_2. When the second interlayer-insulating layer 283 has a thickness of 1.0 μm or more, there is a problem in that the substrate 2 is cracked due to the stress of SiO_2.

[0040]

As shown in FIG. 4, the luminescent power-supply lines

103 have the double wiring structure. The area of each luminescent power-supply line 103 is herein defined as the area of one line (for example, each power supply line $103R_2$, power supply line $103G_2$, or power supply line $103B_2$) included in the double wiring structure.

[0041]

The cathode 12 extending from the display pixel section 3 is disposed above the luminescent power-supply lines 103R. That is, the second lines $103R_2$ of the luminescent power-supply lines 103R are opposed to the cathode 12, with the first interlayer-insulating layer 284 disposed therebetween. This allows the first capacitors C_1 to be formed between the cathode 12 and the second lines $103R_2$.

[0042]

The distance between the second lines $103R_2$ and the cathode 12 is preferably, for example, 0.6 to 1.0 μm. When the distance is smaller than 0.6 μm, the parasitic capacitance between the pixel electrodes and source metals having different potentials is large, thereby causing a wiring delay in signal lines including the source metals. Thus, image signals cannot be written in a predetermined period, thereby causing low contrast. The first interlayer-insulating layer 284 disposed between the second lines $103R_2$ and the cathode 12 is preferably made of, for example, SiO_2, an acrylic resin, or the like. When the first interlayer-

insulating layer 284 is made SiO_2 and has a thickness of 1.0 μm or more, there is a problem in that the substrate 2 is cracked due to the stress. When the first interlayer-insulating layer 284 is made of such an acrylic resin, the first interlayer-insulating layer 284 may have a thickness of up to about 2.0 μm. However, since the acrylic resin expands when it contains moisture, there is a problem in that the pixel electrodes formed on the first interlayer-insulating layer 284 are cracked.

[0043]

As described above, in the electro-optical device 1 of this embodiment, since the first capacitors C_1 are disposed between the luminescent power-supply lines 103 and the cathode 12, charges stored in the first capacitors C_1 are supplied to the luminescent power-supply lines 103 when the potentials of currents flowing in the luminescent power-supply lines 103 fluctuate. That is, the charges compensate for potential shortfalls in driving currents, thereby reducing the potential fluctuation. This allows the electro-optical device 1 to display a normal image. In particular, since the luminescent power-supply lines 103 and the cathode 12 are disposed outside the display pixel section 3 and opposed to each other, the distance between the luminescent power-supply lines 103 and the cathode 12 can be reduced such that charges stored in the first

capacitors C_1 are decreased. This leads to a reduction in the potential fluctuation of driving currents; hence, a stable image can be displayed. Furthermore, the luminescent power-supply lines 103 each have the double wiring structure consisting of the first and second lines and the second capacitors C_2 are disposed between the first lines and the cathode line, charges stored in the second capacitors C_2 are also supplied to the luminescent power-supply lines 103, thereby reducing the potential fluctuation. This allows the electro-optical device 1 to display a normal image.

[0044]

A configuration of the circuit section 11 including the current thin-film transistors 123 will now be described in detail. FIG. 5 is a sectional view showing a principal part of the pixel electrode group region 11a. As shown in FIG. 5, the base-protecting layer 281 principally containing SiO_2 is disposed on the substrate 2 and silicon layers 241 are arranged on the base-protecting layer 281 in a dotted pattern. The silicon layers 241 and the base-protecting layer 281 are covered with a gate-insulating layer 282 principally containing SiO_2 and/or SiN. Gate electrodes 242 are arranged above the silicon layers 241, with the gate-insulating layer 282 disposed therebetween.

[0045]

FIG. 5 shows a cross-sectional structure of each

current thin-film transistor 123. The switching thin-film transistors 112 have the same structure as that of the current thin-film transistors 123. The gate electrodes 242 and the gate-insulating layer 282 are covered with the second interlayer-insulating layer 283 principally containing SiO_2. The term "principal component" is herein defined as a component of which the content is highest.

[0046]

Each silicon layer 241 has a channel region 241a opposed to one of the gate electrodes 242, with the gate-insulating layer 282 disposed therebetween. In the silicon layer 241, a lightly doped source region 241b and a heavily doped source region 241S are disposed on the right side of the channel region 241a. A lightly doped drain region 241c and a heavily doped drain region 241D are disposed on the left side of the channel region 241a and form a so-called LDD (lightly doped drain) structure. The silicon layers 241 are main components of the current thin-film transistors 123.

[0047]

The heavily doped source region 241S is connected to one of source electrodes 243 with one of contact holes 244 extending through the gate-insulating layer 282 and the second interlayer-insulating layer 283. The source electrodes 243 are parts of the above signal lines 102. On the other hand, the heavily doped drain region 241D is

connected to one of drain electrodes 244, disposed on the same level as that of the source electrodes 243, with one of contact holes 245 extending through the gate-insulating layer 282 and the second interlayer-insulating layer 283.

[0048]

The first interlayer-insulating layer 284 is disposed on the second interlayer-insulating layer 283 having the source electrodes 243 and the drain electrodes 244 thereon. The transparent pixel electrodes 111 made of ITO or the like are arranged on the first interlayer-insulating layer 284 and connected to the drain electrodes 244 with contact holes 111a extending through the first interlayer-insulating layer 284. That is, the pixel electrodes 111 are connected to the heavily doped drain regions 241D of the silicon layers 241 with the drain electrodes 245. As shown in FIG. 3, the pixel electrodes 111 are arranged in an area corresponding to the actual display region 4 and dummy pixel electrodes 111' are arranged in the dummy display region 5 surrounding the actual display region 4. The dummy pixel electrodes 111' have substantially the same configuration as that of the pixel electrodes 111 except that each dummy pixel electrode 111' is not connected to the heavily doped drain region 241D.

[0049]

The light-emitting layers 110 and a bank portion (bank)

122 are disposed in the actual display region 4 of the display pixel section 3. As shown in FIGS. 3 to 5, the light-emitting layers 110 are each placed on the corresponding pixel electrodes 111. The bank portion 122 is disposed between the pixel electrodes 111 and the light-emitting layers 110 so as to partition the light-emitting layers 110. The bank portion 122 includes an inorganic bank layer 122a located close to the substrate 2 and an organic bank layer 122b which is located far from the substrate 2 and which is disposed on the inorganic bank layer 112a. A light-shielding layer may be placed between the inorganic bank layer 122a and the organic bank layer 122b.

[0050]

The inorganic bank layer 122a and the organic bank layer 122b extend on end portions of the pixel electrodes 111. The inorganic bank layer 122a extends to a position closer to the center of the circuit section 11 as compared with the organic bank layer 122b. The inorganic bank layer 122a is preferably made of an inorganic material such as SiO_2, TiO_2, or SiN. The inorganic bank layer 122a preferably has a thickness of 50 to 200 nm, and more preferably about 150 nm. When the thickness is smaller than 50 nm, the inorganic bank layer 122a is thinner than hole injection/transport layers described below; hence, the hole injection/transport layers cannot be maintained flat. This

is not preferable. When the thickness is larger than 200 nm, steps due to the inorganic bank layer 122a have a large height; hence, light-emitting layers lying on the hole injection/transport layers cannot be maintained flat. This is not preferable.

[0051]

The organic bank layer 122b is made of an ordinary resist material such as an acrylic resin or a polyimide resin. The organic bank layer 122b preferably has a thickness of 0.1 to 3.5 μm, and more preferably about 2 μm. When the thickness is smaller than 0.1 μm, the thickness of the organic bank layer 122b is less than the sum of the thicknesses of the hole injection/transport layers and the thicknesses of the light-emitting layers. This is not preferable because there is a problem in that the light-emitting layers extend out of upper openings. When the thickness is larger than 3.5 μm, steps disposed at the upper openings have a large height. This is not preferable because the step coverage of the cathode 12 disposed on the organic bank layer 122b cannot be achieved. The organic bank layer 122b preferably has a thickness of about 2 μm because the cathode 12 can be securely insulated from the pixel electrodes 111. That is, the light-emitting layers 110 have a thickness smaller than that of the bank portion 122.

[0052]

Lyophilic regions and a lyophobic region are arranged around the bank portion 122. The lyophilic regions are the inorganic bank layer 122a and the pixel electrodes 111 and have lyophilic groups, such as hydroxyl groups, formed by plasma treatment using oxygen which is a reactive gas. The lyophobic region is the organic bank layer 122b and has lyophobic groups, such as fluorine groups, formed by plasma treatment using tetrafluoromethane which is a reactive gas.

[0053]

As shown in FIG. 5, the light-emitting layers 110 are disposed on the hole injection/transport layers 110a disposed on the pixel electrodes 111. A configuration including each light-emitting layer 110 and each hole injection/transport layer 110a is herein defined as a functional layer, and a configuration including each pixel electrode 111, the functional layer, and the cathode 12 is herein defined as an light-emitting element. The hole injection/transport layer 110a has a function of injecting holes to the light-emitting layer 110 and also has a function of transport holes in the hole injection/transport layer 110a. Since the hole injection/transport layer 110a is disposed between the pixel electrode 111 and the light-emitting layer 110, the light-emitting layer 110 has superior element properties such as high light-emitting

efficiency and long life. In the light-emitting layer 110, fluorescence occurs when holes injected from the hole injection/transport layer 110a combine with electrons supplied from the cathode 12. The light-emitting layers 110 include three types of layers: light-emitting layers for emitting red light (R), light-emitting layers for emitting green light (G), and light-emitting layers for emitting blue light (B). As shown in FIGS. 1 and 2, these layers are arranged in a striped pattern.

[0054]

As shown in FIGS. 3 and 4, the dummy region 5 of the display pixel section 3 includes dummy light-emitting layers 210 and a dummy bank portion 212. The dummy bank portion 212 includes a dummy inorganic bank layer 212a located close to the substrate 2 and a dummy organic bank layer 212b which is located far from the substrate 2 and which is disposed on the dummy inorganic bank layer 212a. The dummy inorganic bank layer 212a lies over the dummy pixel electrodes 111'. The dummy organic bank layer 212b, as well as the organic bank layer 122b, is disposed between the pixel electrodes 111. The dummy light-emitting layers 210 are arranged above the dummy pixel electrodes 111', with the dummy inorganic bank layer 212a disposed therebetween.

[0055]

The dummy inorganic bank layer 212a and the inorganic

bank layer 122a described above are made of the same material and have the same thickness and the dummy organic bank layer 212b and the organic bank layer 122b described above are made of the same material and have the same thickness. The dummy light-emitting layers 210 are disposed on dummy hole injection/transport layers, which are not shown. The dummy hole injection/transport layers and the hole injection/transport layers 110a are made of the same material and have the same thickness. The dummy light-emitting layers and the light-emitting layers 110 are made of the same material and have the same thickness. Thus, the dummy light-emitting layers 210, as well as the light-emitting layers 110, have a thickness smaller than that of the dummy bank portion 212.

[0056]

Since the dummy region 5 is placed around the actual display region 4, the light-emitting layers 110 in the actual display region 4 have a uniform thickness, thereby preventing uneven display. That is, since the dummy region 5 is present, an ejected ink composition can be dried under constant conditions in the actual display region 4 if the display elements are formed by an inkjet process. This prevents the light-emitting layers 110 located close to ends of the actual display region 4 from having uneven thickness.

[0057]

The cathode 12 extends over the actual display region 4 and the dummy region 5 and further extends to positions above the substrate 2, the positions being disposed outside the dummy region 5. At the outside of the dummy region 5, that is, at the outside of the display pixel section 3, the cathode 12 is opposed to the luminescent power-supply lines 103. End portions of the cathode 12 are connected to the entire cathode line 12a. The cathode 12 acts as a counter electrode for the pixel electrodes 111 and has a function of applying currents to the light-emitting layers 110. The cathode 12 includes a cathode layer 12b including, for example, a lithium fluoride sub-layer and a calcium sub-layer and also includes a reflective layer 12c. In the cathode 12, only the reflective layer 12c extends outside the display pixel section 3. The reflective layer 12c has a function of reflecting light, emitted from the light-emitting layers 110, toward the substrate 2 and is preferably comprises, for example, Al, Ag, or an Mg/Ag layered structure. A protective layer, made of SiO_2, SiN, or the like, for preventing oxidation may be placed on the reflective layer 12c.

[0058]

A method for manufacturing the electro-optical device 1 of this embodiment will now be described. FIGS. 6 to 9 are illustrations showing steps included in an electro-optical

device manufacturing method according to an embodiment of the present invention. A procedure for forming the circuit section 11 on the substrate 2 is described below with reference to FIGS. 6 to 8. FIGS. 6 to 8 are sectional views taken along the line A-A' of FIG. 2. In the following description, impurity concentrations determined after activation annealing are used.

[0059]

As shown in FIG. 6(a), the base-protecting layer 281 comprising a silicon oxide film or the like is formed on the substrate 2. An amorphous silicon layer is formed thereon by an ICVD process, a plasma CVD process, or another process and then converted into a polysilicon layer 501 in such a manner that crystal grains are grown by a laser annealing process or a rapid heating process. As shown in FIG. 6(b), the polysilicon layer 501 is patterned by a photolithographic process such that the silicon layers 241 and silicon layers 251 and 261 are formed in a dotted pattern. The gate-insulating layer 282 comprising a silicon oxide film is then formed thereon.

[0060]

The silicon layers 241 are components of the current thin-film transistors 123 (hereinafter referred to as "pixel TFTs" in some cases) which is disposed at a position corresponding to the actual display region 4 and which is

connected to each pixel electrode 111. The silicon layer 251 and 261 are components of p-channel type thin-film transistors and n-channel type thin-film transistors (hereinafter referred to as "driving circuit TFTs" in some cases) included in the scanning driving circuits 105.

[0061]

The gate-insulating layer 282 is formed by a plasma CVD process, a thermal oxidation process, or the like such that a silicon dioxide layer covers the silicon layers 241, 251, and 261 and the base-protecting layer 281 and has a thickness of about 30 to 200 nm. If the gate-insulating layer 282 is formed by the thermal oxidation process, the silicon layers 241, 251, and 261 can be crystallized, thereby converting these silicon layers into polysilicon layers. In order to perform channel doping, for example, boron ions are implanted at a dose of about 1×10^{12} cm^{-2} in the above operation. As a result, the silicon layers 241, 251, and 261 are converted into lightly doped p-type silicon layers having an impurity concentration of about 1×10^{-17} cm^{-3}.

[0062]

As shown in FIG. 6(c), ion-implanting selection masks M_1 are formed on portions of the silicon layers 241 and 261 and phosphorus ions are then implanted at a dose of about 1×10^{15} cm^{-2}. As a result, a large amount of dopants are

introduced into the silicon layers such that the dopants are self-aligned with respect to the ion-implanting selection masks M_1, whereby the heavily doped source regions 241S and 261S and the heavily doped drain regions 241D and 261D are formed in the silicon layers 241 and 261.

[0063]

As shown in FIG. 6(d), after the ion-implanting selection masks M_1 are removed, doped silicon layers, silicide layers, or metal layers such as aluminum layers, chromium layers, or tantalum layers are formed on the gate-insulating layer 282 so as to have a thickness of about 200 nm. The layers are then patterned, thereby forming gate electrodes 252 of p-channel type TFTs for driving circuits, the gate electrodes 242 of pixel TFTs, and gate electrodes 262 of n-channel type TFTs for driving circuits. During the patterning step, the following lines are simultaneously formed: the scanning line-driving circuit control signal lines 105a, the first lines $103R_1$, $103G_1$, and $103B_1$ of the luminescent power-supply lines, and a portion of the cathode line 12a.

[0064]

Phosphorus ions are then implanted into the silicon layers 241, 251, and 261 at a dose of about 4×10^{13} cm^{-2} using the gate electrodes 242, 252, and 262 as masks. As a result, a small amount of dopants are introduced into the

silicon layers such that the dopants are self-aligned with respect to the gate electrodes 242, 252, and 262, whereby the lightly doped source regions 241b and 261b and the lightly doped drain regions 241c 261c are formed in the silicon layers 241 and 261 as shown in FIG. 6(d). Furthermore, lightly doped source regions 251S and 251D are formed in the silicon layers 251.

[0065]

As shown in FIG. 7(a), an ion-implanting selection mask M_2 is formed over the substrate 2 other than the vicinities of the gate electrodes 252. Boron ions are then implanted into the silicon layers 251 at a dose of about 1.5×10^{15} cm^{-2} using the ion-implanting selection mask M_2. Since the gate electrodes 252 also function as masks, the silicon layers 251 are heavily doped with dopants in a self-aligned manner. Thereby, the lightly doped source regions 251S and 251D are counter-doped, so that the lightly doped source regions 251S and 251D function as source regions and drain regions of the p-channel type TFTs for the driving circuits.

[0066]

As shown in FIG. 7(b), after the ion-implanting selection mask M_2 is removed, the second interlayer-insulating layer 283 is formed over the substrate 2. The second interlayer-insulating layer 283 is then patterned by a lithographic process, whereby openings H_1 for forming

contact holes are formed at positions corresponding to the cathode line 12a and the source and drain electrodes of the TFTs. As shown in FIG. 7(c), a conductive layer 504, made of metal such as aluminum, chromium, or tantalum, having a thickness of about 200 to 800 nm is formed over the second interlayer-insulating layer 283, whereby the openings H_1 is filled with the metal such that contact holes are formed. Patterning masks M_3 are then formed on the conductive layer 504.

[0067]

As shown in FIG. 8(a), the conductive layer 504 is patterned using the patterning masks M_3, whereby the following electrodes and lines are formed: the source electrodes 243, 253, and 263 and drain electrodes 244 and 254 of the TFTs; the second lines $103R_2$, $103G_2$, and $103B_2$ of the luminescent power-supply lines; the scanning line-driving circuit power-supply lines 105b; and the cathode line 12b. According to the above configuration, the first lines $103R_1$ and $103B_1$ and the cathode line 12a are arranged on the same level, whereby the second capacitors C_2 are formed.

[0068]

After the above steps are finished, as shown in FIG. 8(b), the first interlayer-insulating layer 284 made of, for example, a resin material such as an acrylic material is

formed over the second interlayer-insulating layer 283. The first interlayer-insulating layer 284 preferably has a thickness of about 1 to 2 μm. As shown in FIG. 8(c), portions of the first interlayer-insulating layer 284 that correspond to the contact holes 244 of the pixel TFTs are removed by an etching process, whereby openings H_2 for forming contact holes are formed. In this procedure, the first interlayer-insulating layer 284 lying over the cathode line 12a is also removed. According to this procedure, the circuit section 11 is formed on the substrate 2.

[0069]

The following procedure will now be described with reference to FIG. 9: a procedure for forming the display pixel section 3 on the circuit section 11 to obtain the electro-optical device 1. FIG. 9 is a sectional view taken along the line A-A' of FIG. 2. As shown in FIG. 9(a), a thin-film made of a transparent electrode material such as ITO is formed over the substrate 2 and then patterned, whereby the pixel electrodes 111 and the dummy pixel electrodes 111' are formed and the openings H_2 formed in the first interlayer-insulating layer 284 are filled with the material such that the contact holes 111a are formed. The pixel electrodes 111 are formed only in an area for forming the current thin-film transistors 123 (switching elements) and connected to the current thin-film transistors 123 with

the contact holes 111a. The dummy pixel electrodes 111' are arranged in a dotted pattern.

[0070]

As shown in FIG. 9(b), the inorganic bank layer 122a and the dummy inorganic bank layer 212a are formed over the first interlayer-insulating layer 284, the pixel electrodes 111, and the dummy pixel electrode 111'. The inorganic bank layer 122a has openings located above the pixel electrodes 111 and the dummy inorganic bank layer 212a completely covers the dummy pixel electrode 111'. The inorganic bank layer 122a and the dummy inorganic bank layer 212a are formed in such a manner that an inorganic layer made of SiO_2, TiO_2, SiN, or the like is formed over the first interlayer-insulating layer 284 and the pixel electrodes 111 by a CVD process, a TEOS process, a sputtering process, or a vapor deposition process and then patterned.

[0071]

Furthermore, as shown in FIG. 9(b), the organic bank layer 122b and the dummy organic bank layer 212b are formed on the inorganic bank layer 122a and the dummy inorganic bank layer 212a, respectively. The organic bank layer 122b disposed on the inorganic bank layer 122a has openings located above the pixel electrodes 111 and the dummy organic bank layer 212b has openings from which parts of the dummy inorganic bank layer 212a are exposed. According to this

procedure, the bank portion 122 is formed on the first interlayer-insulating layer 284.

[0072]

The lyophilic regions and the lyophobic regions are formed on the bank portion 122. In this embodiment, these regions are formed by a plasma-treating process. In particular, the plasma-treating process includes at least a lyophilizing step of lyophilizing the pixel electrodes 111, the inorganic bank layer 122a, and the dummy inorganic bank layer 212a and a lyophobing step of lyophobing the organic bank layer 122b and the dummy organic bank layer 212b.

[0073]

The bank portion 122 is heated to a predetermined temperature (for example, about 70 to 80°C) and then subjected to plasma treatment (O_2 plasma treatment) using oxygen as reactive gas in an air atmosphere in the lyophilizing step. Subsequently, plasma treatment (CF_4 plasma treatment) using tetrafluoromethane as reactive gas is performed in an air atmosphere in the lyophobing step and the bank portion 122 heated due to the plasma treatment is then cooled to room temperature, whereby predetermined sections are rendered lyophilic or lyophobic.

[0074]

The light-emitting layers 110 and the dummy light-emitting layers 210 are formed on the pixel electrodes 111

and the dummy inorganic bank layer 112a, respectively, by an inkjet process. The light-emitting layers 110 and the dummy light-emitting layers 210 are formed by the following procedure: an ink composition containing a hole injection/transport material is discharged and then dried and another ink composition containing a light-emitting material is discharged and then dried. In order to prevent the hole injection/transport layers and the light-emitting layers from being oxidized, steps subsequent to the step of forming the light-emitting layers 110 and the dummy light-emitting layers 210 are preferably performed in an inert-gas atmosphere such as a nitrogen atmosphere or an argon atmosphere.

[0075]

As shown in FIG. 9(c), the cathode 12 is formed so as to cover the bank portion 122, the light-emitting layers 110, and the dummy light-emitting layers 210. The cathode 12 is formed in such a manner that the cathode layer 12b is formed over the bank portion 122, the light-emitting layers 110, and the dummy light-emitting layers 210 and the reflective layer 12c connected to the cathode line 12a disposed above the substrate 2 is then formed over the cathode layer 12b. Since the reflective layer 12c extends from the display pixel section 3 to portions above the substrate 2 such that the reflective layer 12c is connected to the cathode line

12a, the reflective layer 12c is opposed to the luminescent power-supply lines 103, with the first interlayer-insulating layer 284 disposed therebetween. Hence, the first capacitors C_1 are formed between the luminescent power-supply lines 103 and the reflective layer 12c. Finally, the substrate 2 is coated with the sealing member 13 containing an epoxy resin or the like and the sealing substrate 14 is then joined to the substrate 2 with the sealing member 13 disposed therebetween. According to the above procedure, the electro-optical device 1 shown in FIGS. 1 to 4 is obtained.

[0076]

For example, a notebook-type personal computer (electronic apparatus) 600 shown in FIG. 10 is manufactured by installing electronic components, such as an electro-optical device manufactured by the above procedure, a keyboard, a hard disk, and a motherboard including a central processing unit (CPU), in a casing. FIG. 10 is an illustration showing an exemplary electronic apparatus including an electro-optical device according to an embodiment of the present invention. In FIG. 10, reference numeral 601 represents a casing, reference numeral 602 represents a liquid crystal display unit, and reference numeral 603 represents a keyboard. FIG. 11 is a perspective view showing a mobile phone which is another electronic

apparatus. The mobile phone 700 shown in FIG. 11 includes an antenna 701, a receiver 702, a microphone 703, a liquid crystal display unit 704, and an operating button section 705.

[0077]

In the above embodiment, the notebook-type personal computer and the mobile phone are described as examples of electronic apparatuses. However, the present invention is not limited to such apparatuses and covers other electronic apparatuses such as liquid crystal projectors, multimedia personal computers (PCs), multimedia engineering work stations (EWSs), pagers, word processors, televisions, viewfinder-type or direct view-type video tape recorders, electronic notebooks, portable electronic calculators, car navigation systems, POS terminals, touch panel-including apparatuses.

[0078]

[Advantages]

As described above, according to the present invention, a cathode line has an area larger than that of each power-supply line such that the cathode line has a small wiring resistance. Therefore, there is an advantage in that the voltage drop in the cathode line can be reduced when currents supplied from the power-supply lines to light-emitting elements through first electrodes flow in the

cathode line. This leads to an advantage that image signals can be reliably transmitted such that a wrong image such as a low-contrast image is prevented from being displayed.

[Brief Description of the Drawings]

[FIG. 1] FIG. 1 is a schematic view showing a wiring structure of an electro-optical device according to an embodiment of the present invention.

[FIG. 2] FIG. 2 is a schematic plan view of the electro-optical device.

[FIG. 3] FIG. 3 is a sectional view taken along the line A-A' of FIG. 2.

[FIG. 4] FIG. 4 is a sectional view taken along the line B-B' of FIG. 2.

[FIG. 5] FIG. 5 is a sectional view showing a principal part of a pixel electrode group region 11a.

[FIG. 6] FIG. 6 is an illustration showing steps included in a method for manufacturing an electro-optical device according to an embodiment of the present invention.

[FIG. 7] FIG. 7 is an illustration showing steps included in the manufacturing method.

[FIG. 8] FIG. 8 is an illustration showing steps included in the manufacturing method.

[FIG. 9] FIG. 9 is an illustration showing steps included in the manufacturing method.

[FIG. 10] FIG. 10 is an illustration showing an exemplary

electronic apparatus including an electro-optical device according to an embodiment of the present invention.

[FIG. 11] FIG. 11 is a perspective view showing a mobile phone which is another electronic apparatus.

[FIG. 12] FIG. 12 is a wiring diagram of a known electro-optical device.

[Reference Numerals]

4: actual display region (effective display region)

5: dummy region

12: cathode (second electrode)

12a: cathode line

101: scanning lines (control lines)

102: signal lines (control lines)

103, 103R, 103G, and 103B: luminescent power-supply lines

110, 110R, 110G, and 110B: light-emitting elements

110a: hole injection/transport layers

110: light-emitting layers

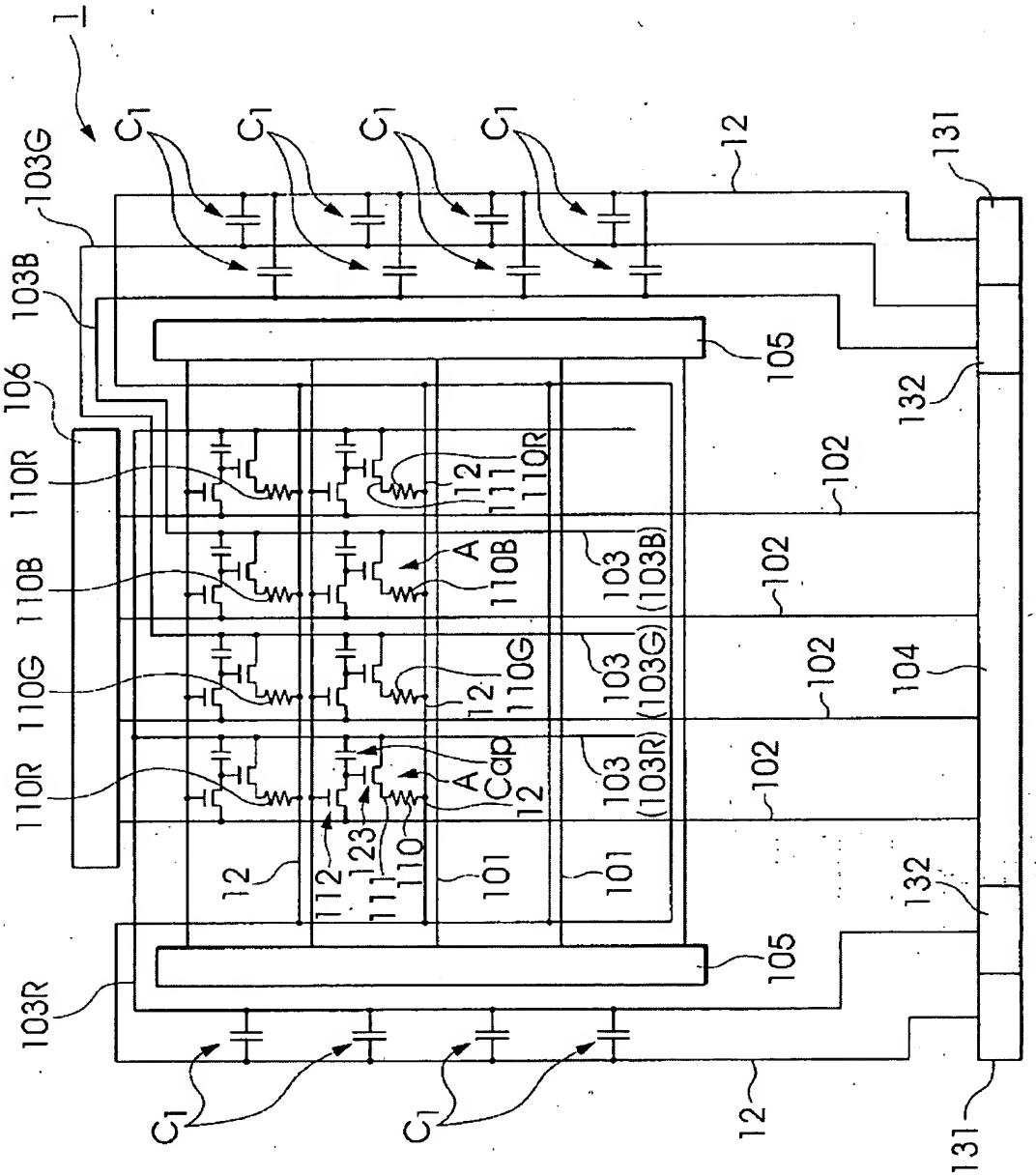
111: pixel electrodes (first electrodes)

112: switching thin-film transistors (switching elements)

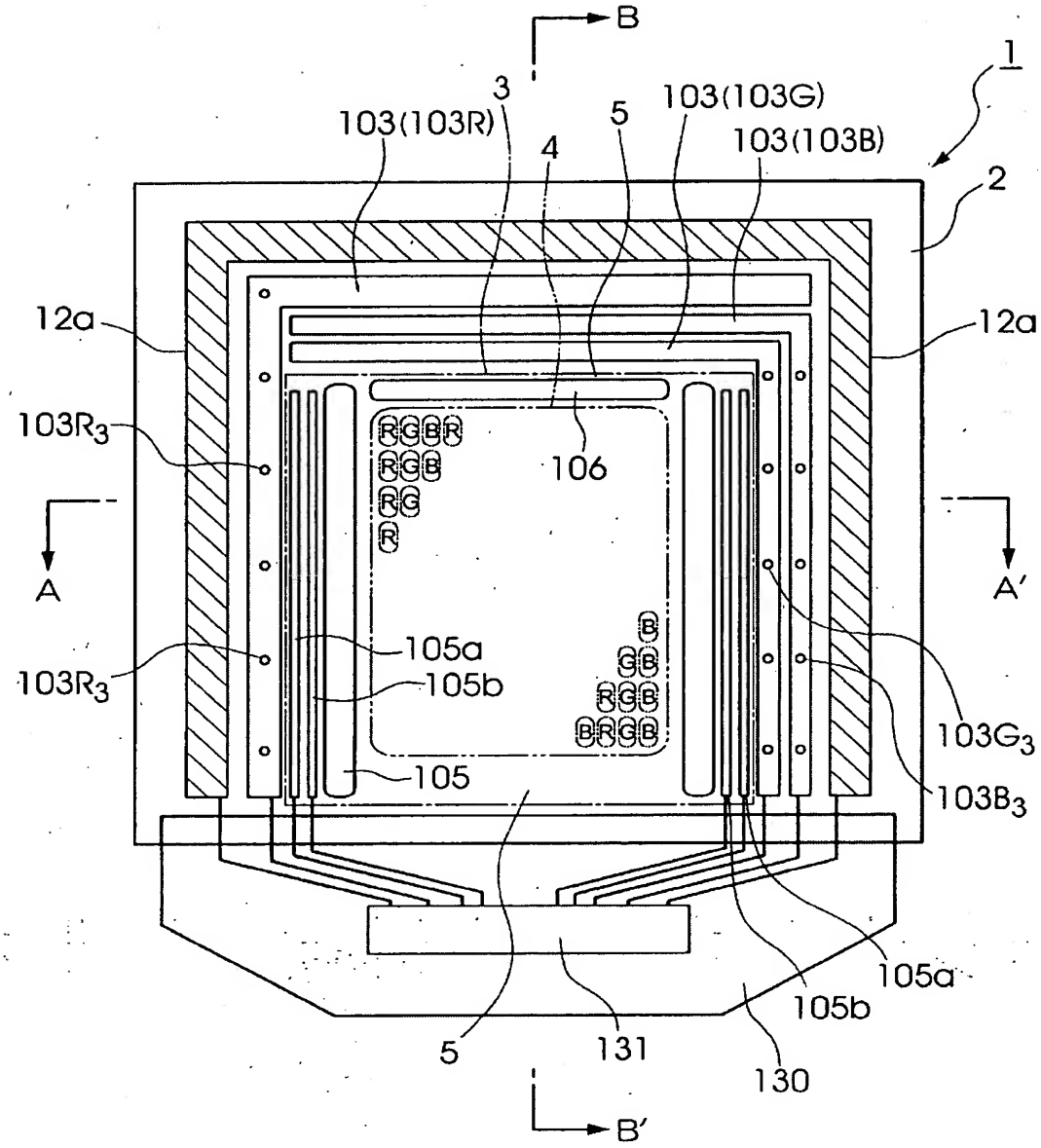
123: current thin-film transistors (switching elements)

[Name of Document] DRAWINGS

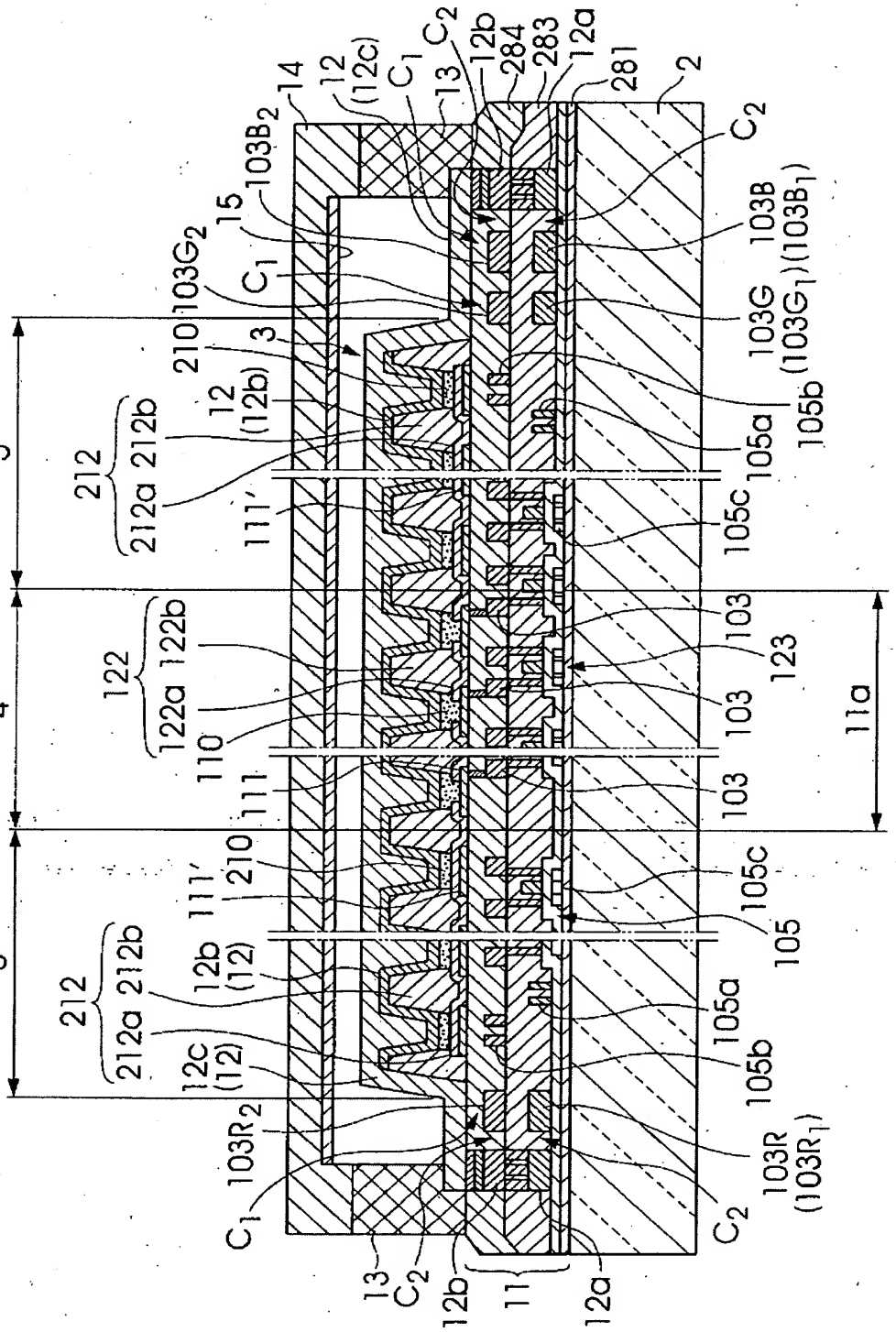
[FIG. 1]



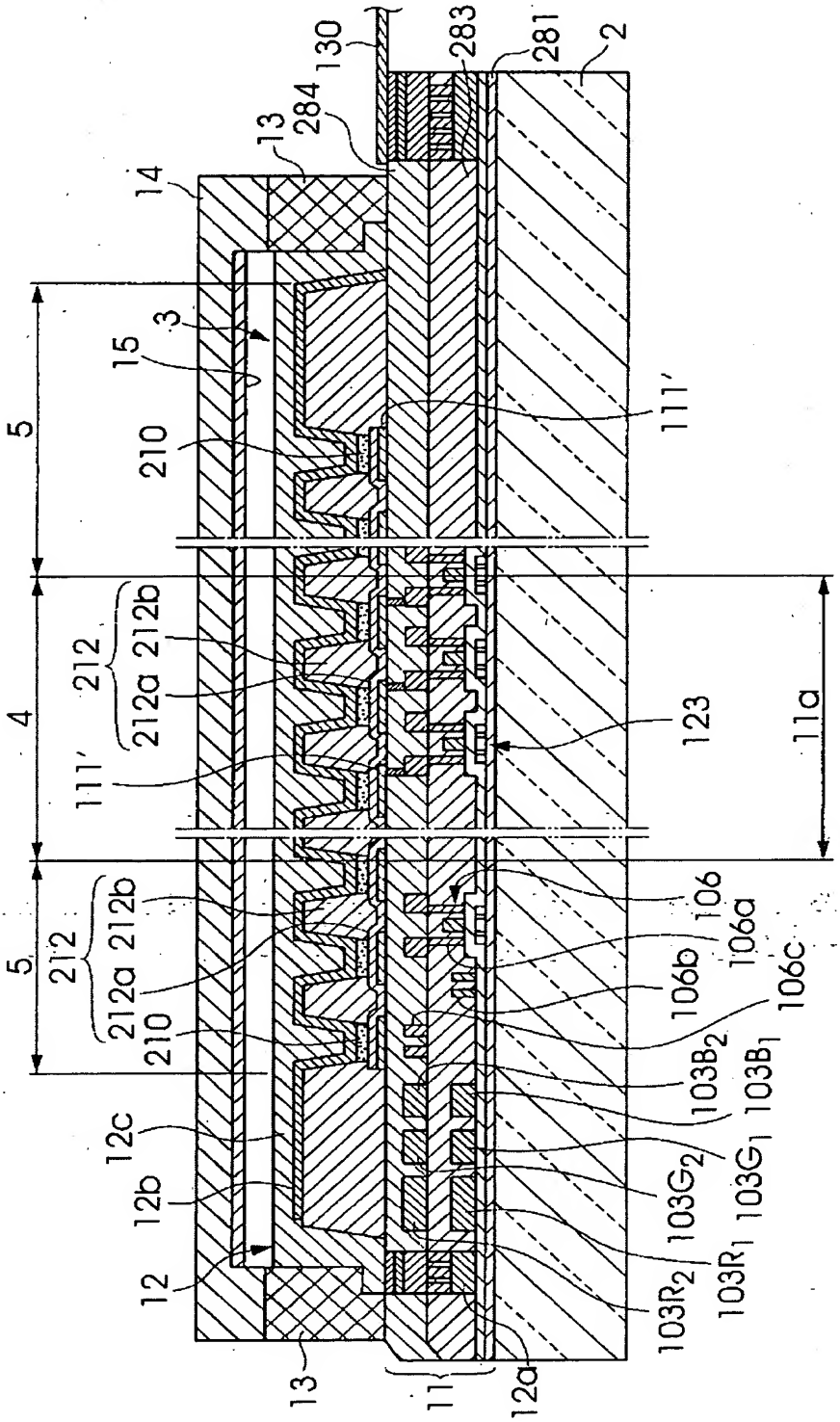
[FIG. 2]


B
1
3
103(103R)
4
5
103(103G)
103(103B)
2
12a
12a
103R3
106
A
A'
105a
103R3
105b
103G3
103B3
105
105a
105b
5
131
130
B'

[FIG. 3]


5
4
5
11a
2
281
283
284
12b
12a
13
14
15
12
(12c)
C_1
C_2
$103B_2$
$103G_2$
$103R_2$
210
3
212
212a
212b
12
(12b)
111'
111
110
122
122a
122b
103
123
105
105a
105b
105c
103G
103B
103R
$(103G_1)$
$(103B_1)$
$(103R_1)$
11

[FIG. 4]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283
281
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284
13
14
3
15
5
210
111'
4
212
212b
212a
123
11a
106
106a
106b
106c
$103B_2$
$103B_1$
$103G_2$
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$103R_1$
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12b
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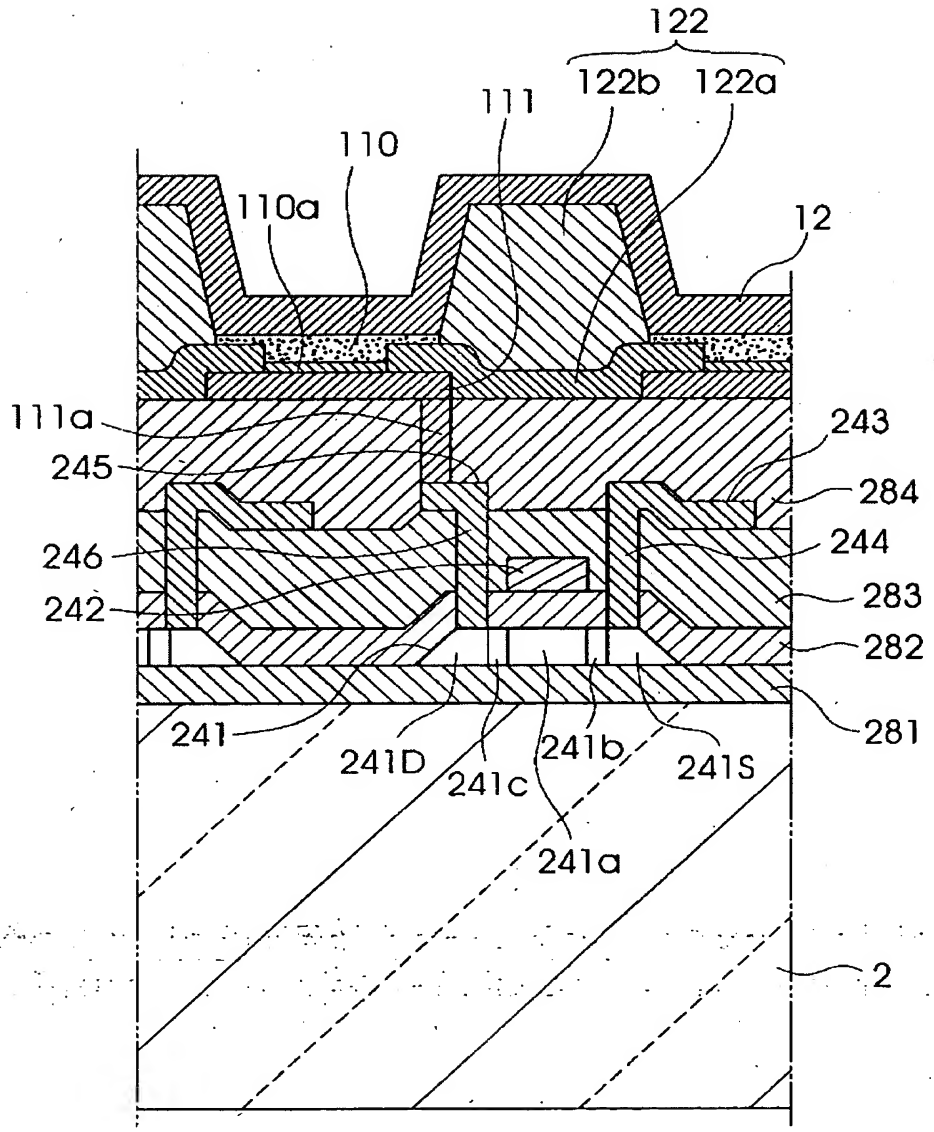
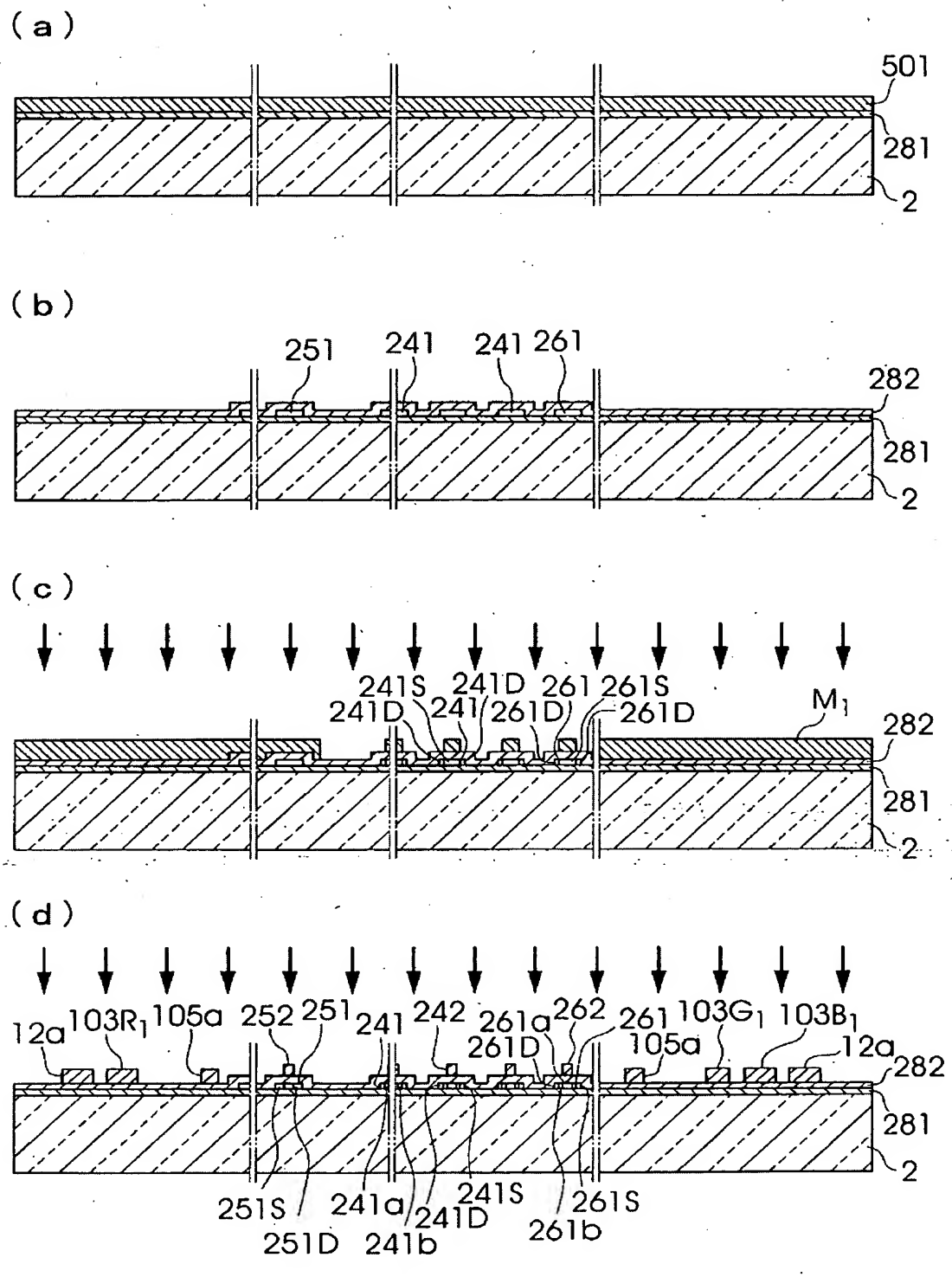
13
11
12a

[FIG. 5]

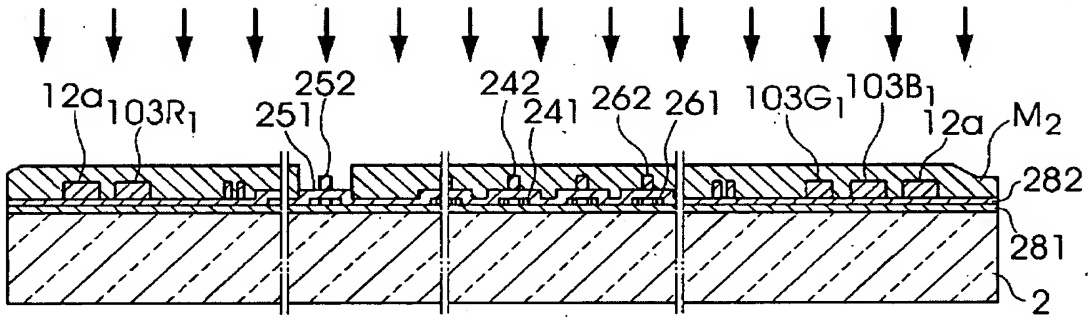

122
122b
122a
111
110
110a
12
111a
245
243
284
246
244
242
283
282
241
281
241D
241c
241b
241S
241a
2

[FIG. 6]

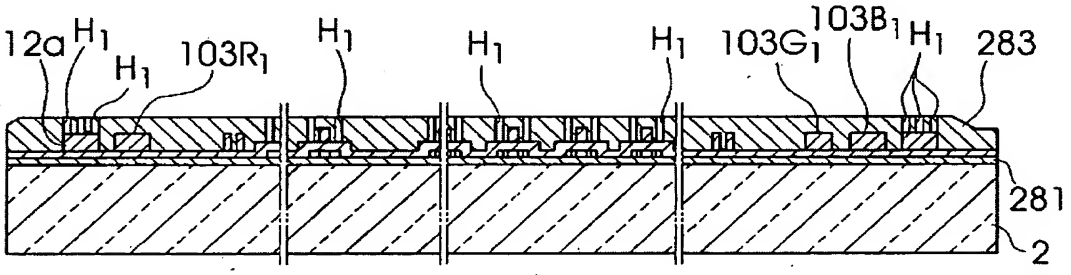

(a)
501
281
2
(b)
251
241
241
261
282
281
2
(c)
241S
241D
241D
241
261
261D
261S
261D
M1
282
281
2
(d)
12a
103R1
105a
252
251
241
242
261a
261D
262
261
105a
103G1
103B1
12a
282
281
2
251S
251D
241a
241b
241D
241S
261b
261S

[FIG. 7]

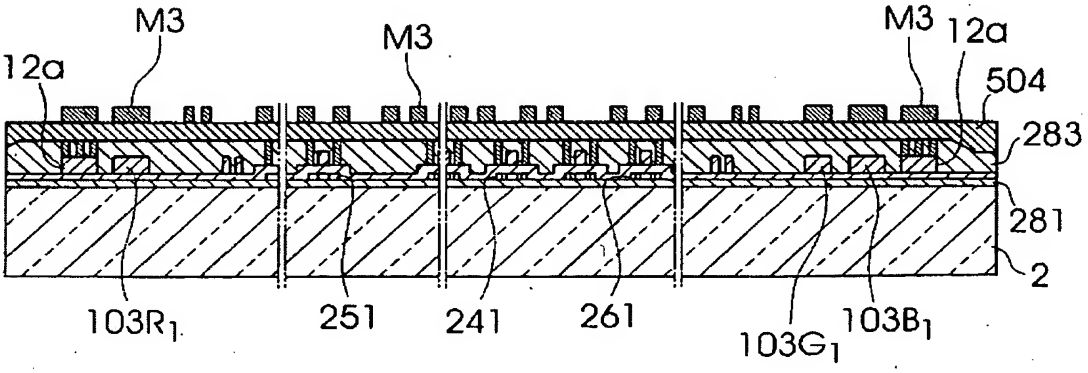
(a)


12a
103R1
251
252
242
241
262
261
103G1
103B1
12a
M2
282
281
2

(b)

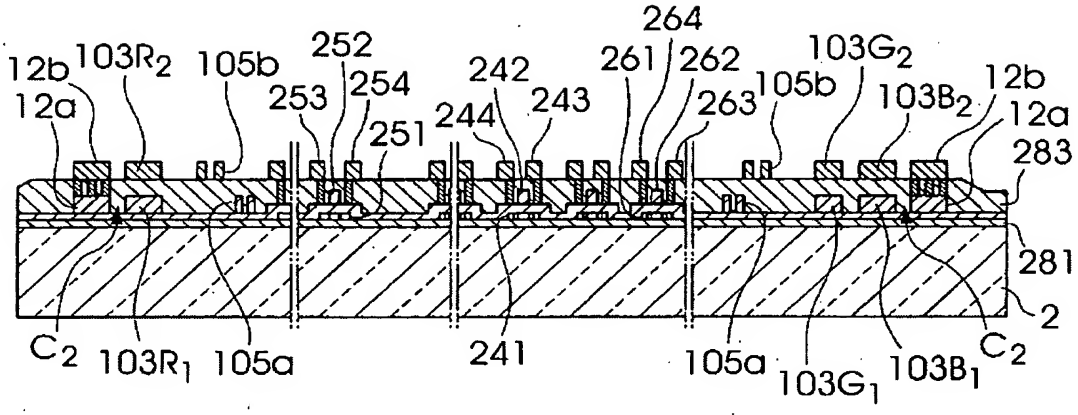

12a
H1
H1
103R1
H1
H1
H1
103G1
103B1
H1
283
281
2

(c)

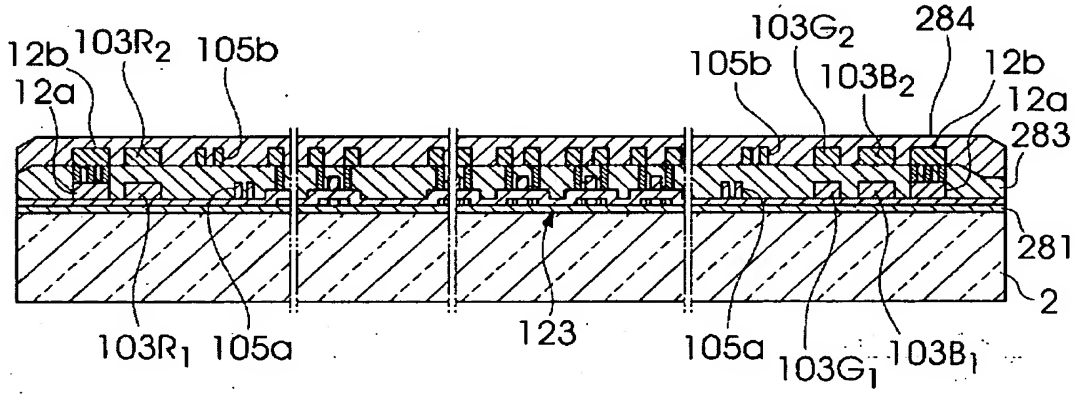

M3
12a
M3
M3
12a
504
283
281
2
103R1
251
241
261
103G1
103B1

[FIG. 8]

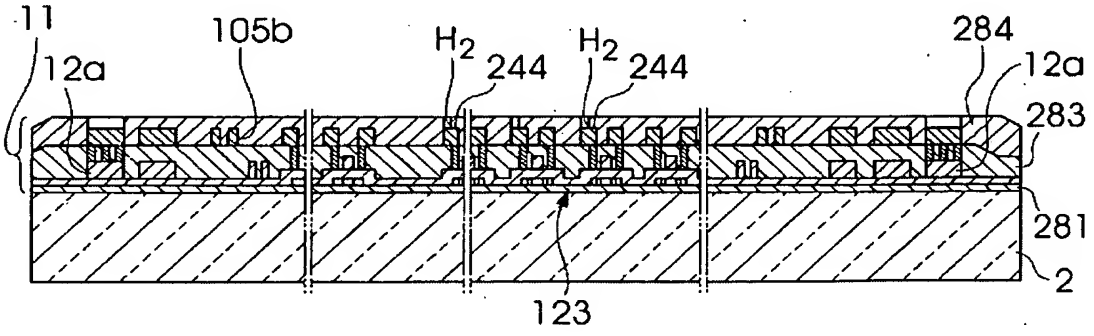
(a)


12b
12a
103R2
105b
252
253
254
251
242
244
243
264
261
262
263
105b
103G2
103B2
12b
12a
283
281
2
C2
103R1
105a
241
105a
103G1
103B1
C2

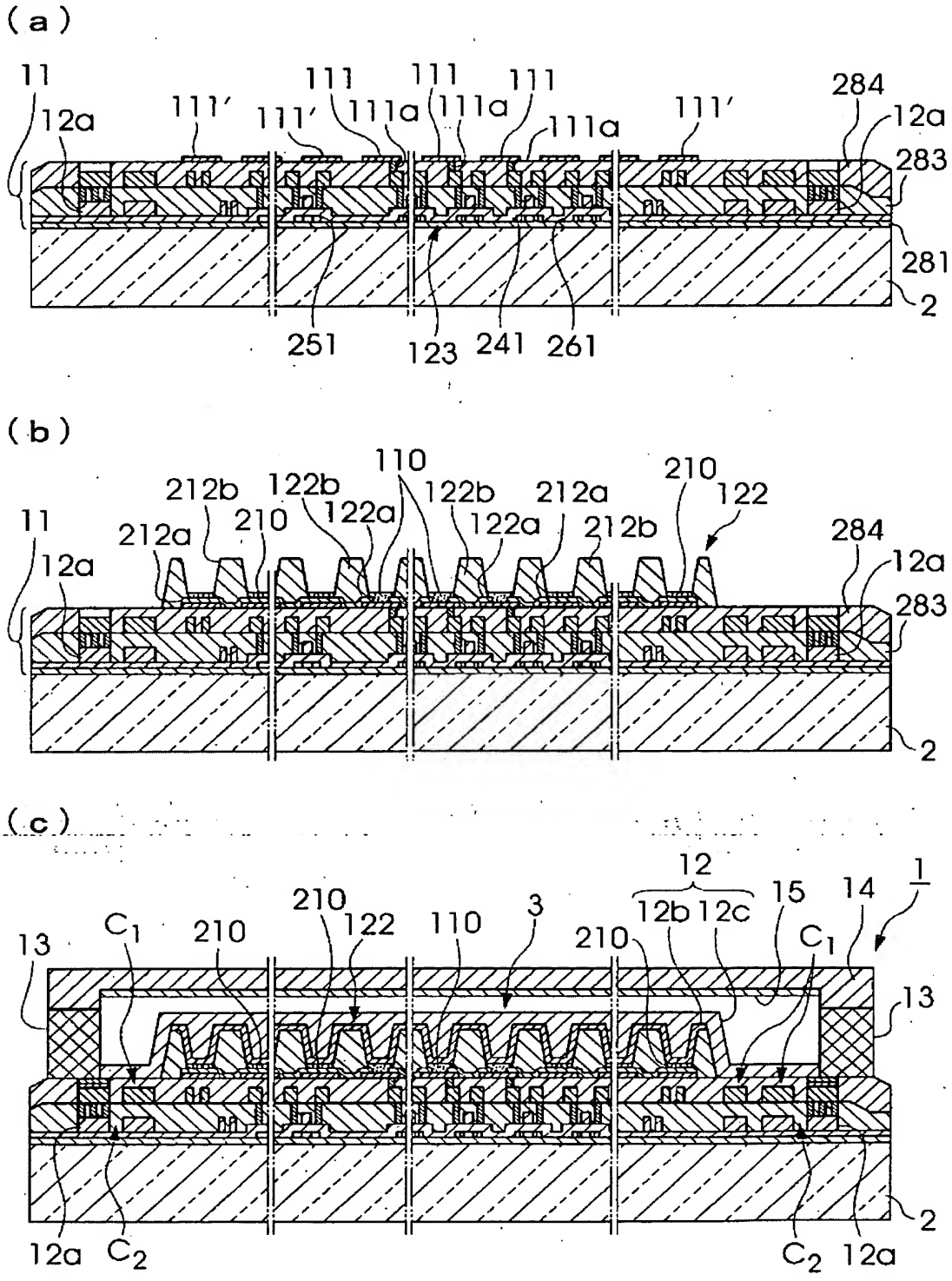
(b)


12b
12a
103R2
105b
103G2
105b
103B2
284
12b
12a
283
281
2
103R1
105a
123
105a
103G1
103B1

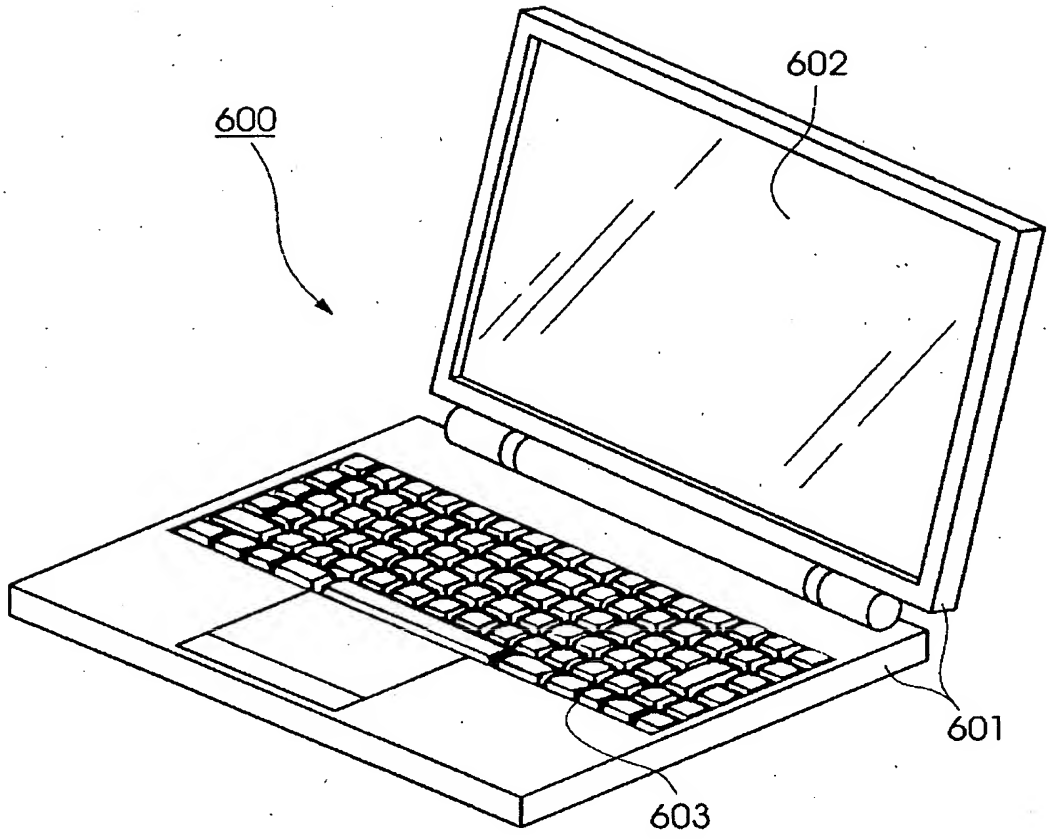
(c)


11
12a
105b
H2
244
H2
244
284
12a
283
281
2
123

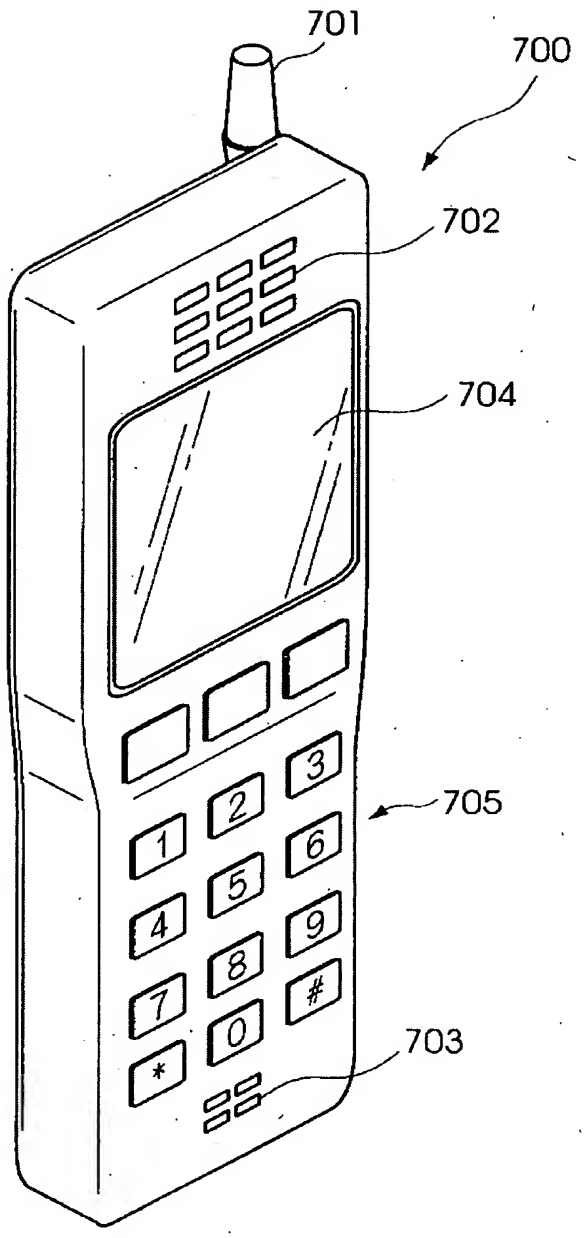
[FIG. 9]


(a)
11
12a
111'
111'
111
111a
111
111a
111a
111'
284
12a
283
281
2
251
123
241
261
(b)
11
12a
212a
212b
210
122b
122a
110
122b
122a
212a
212b
210
122
284
12a
283
2
(c)
13
C1
210
210
122
110
3
210
12
12b
12c
15
C1
14
1
13
12a
C2
C2
12a
2

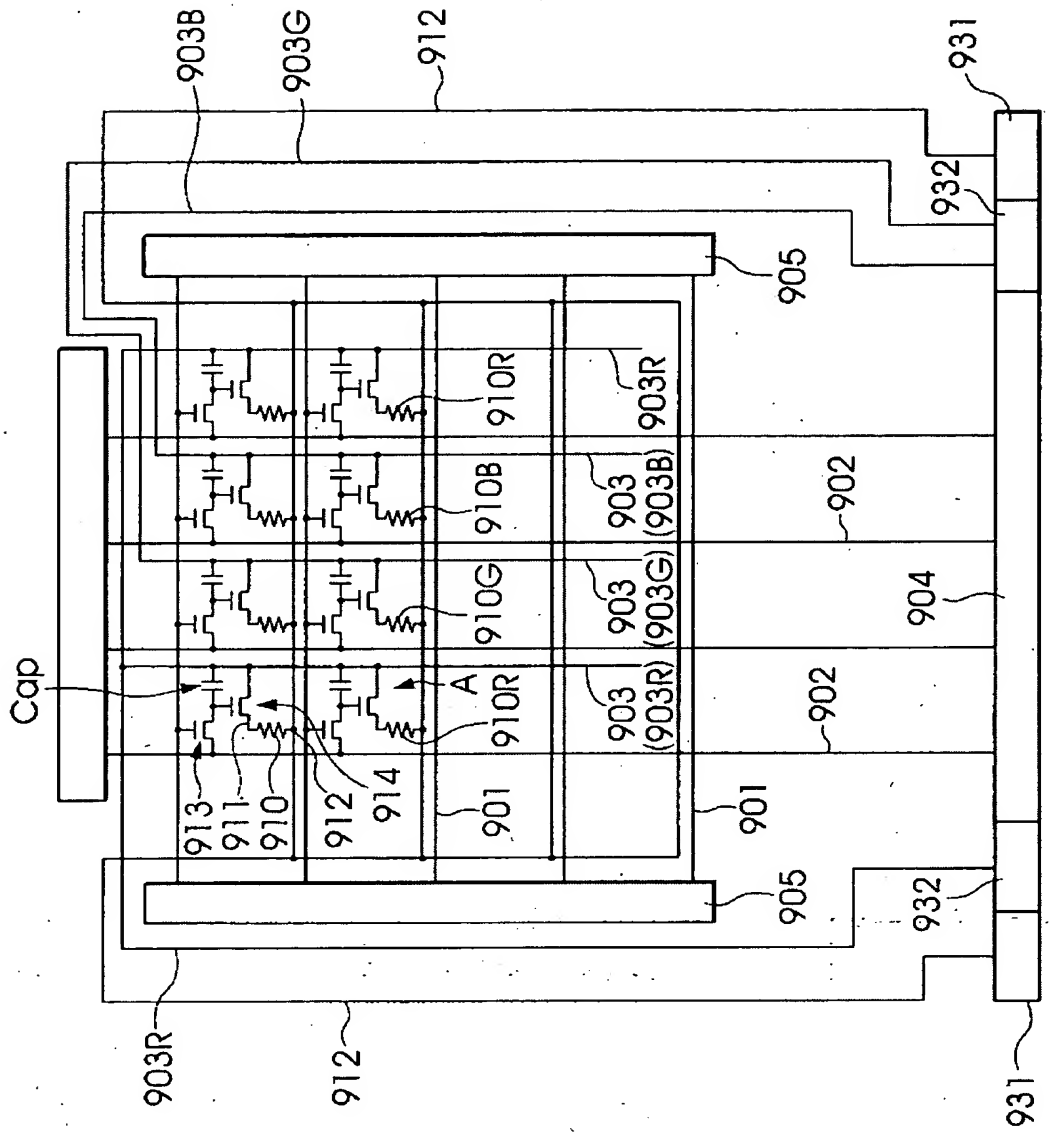
[FIG. 10]



[FIG. 11]



[FIG. 12]


903B
903G
912
931
932
905
910R
903R
903
(903B)
902
910B
903
(903G)
904
910G
Cap
903
(903R)
902
A
910R
913
911
910
912
914
901
901
905
932
903R
912
931

[Name of Document] ABSTRACT

[Abstract]

[Object] To provide a electro-optical device in which image signals are reliably transmitted by reducing the voltage drop due to the wiring resistance of a cathode such that a wrong image such as a low-contrast image is prevented from being displayed and also provide a electronic apparatus including the electro-optical device.

[Solving Means] An actual display region 4 contains luminescent power-supply lines 103R, 103G, and 103B for supplying currents to light-emitting elements arranged in a matrix and also contains a cathode line 12a disposed between the light-emitting elements and the cathode. The cathode line 12a has a width larger than that of each of the luminescent power-supply lines 102R, 102G, and 102B.

[Selected Figure] FIG. 2